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EXAMINER	
LEE, CHUN KUAN	

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2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/807,968	THOMAS, DAVID	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-10 and 12-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-10 and 12-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Fish et al. (US Patent 4,241,420). Rejection of claim 12-14 under 35 U.S.C. 112 first paragraph is withdrawn. Currently, claims 6 and 11 is canceled and claims 1-5, 7-10 and 12-14 are pending for examination.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

III. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4-5, 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Grady et al. (US Patent 6,757,791) in view of Jaquette et al. (US Patent 6,009,547) and Fish et al. (US Patent 4,241,420).

5. As per claims 1 and 12, O'Grady teaches a data buffering system and method comprising:

allocating a plurality of blocks of storage (Fig. 2, ref. 161) in a memory (Fig. 2, ref. 160) in a buffering device for storing a transfer length of unblock data (Abstract; col. 1, ll. 23-29; col. 1, l. 63 to col. 2, l. 17 and col. 6, ll. 36-43), wherein the packet (Fig. 2, ref. 113) of different transfer length are received, disassembled into cells to be stored into the plurality of blocks of storage as allocated;

receiving a data (e.g. packet) on a first port (Fig. 1, ref. 111) from a source, said source determining said transfer length (Fig. 1-2 and col. 1, ll. 23-29), wherein the transfer length corresponds to the type of packet received, and that different source would transfer different packet having different length, therefore the transfer length of the packet would depend on the source transferring the packet;

writing said data, as said data is received, to successive ones of said plurality of blocks until an end of said transfer length is reached (col. 1, l. 63 to col. 2, l. 17 and col.

6, ll. 36-43), as the packets of different length are received, disassembled into cells and stored (i.e. written) into the corresponding first-in-first-out (FIFO) queues in the plurality of blocks successively till the end of the packet; and

writing said data to a second port (Fig. 2, ref. 112) from the memory bank (col. 6, l. 47 to col. 7, l. 8).

O'Grady does not teach a method and a computer program product stored on a computer readable medium to be executed for protecting data as it passes through a buffering device that connects protocols that use different block sizes or unblocked data, comprising:

wherein each one of said plurality of blocks having a length of 2^n, where n is a positive integer;

if an end one of said plurality of blocks that includes an end of said transfer length is not full of data, adding padding to said end one of said plurality of blocks until said end one of said plurality of blocks is completed, wherein padding is added only to an end one of said plurality of blocks that includes an end of said transfer length until the end one of the plurality of block is complete;

as said data is being written to each one of said plurality of blocks, calculating a running cyclical redundancy code (CRC) for each of said plurality of blocks;

when writing to each one of said plurality of blocks is completed, storing, for each one of said plurality of blocks, a final value of said running CRC that was calculated for each one of said plurality of blocks as a first CRC in a second memory on said buffering device; and

when writing said data to a second port, computing a second CRC for each of said plurality of blocks and if said second CRC corresponding to a given block is equal to said first CRC corresponding to said given block, writing said given block to said second port.

Jaquette teaches a method and a computer program product stored on a computer readable medium to be executed for protecting data as it passes through a buffering device (Fig. 1, ref. 10, 16) that connects protocols that use different block sizes or unblocked data (col. 4, ll. 8-50, wherein the data received from the host system is unblocked as padding may be utilized to form blocks of data), comprising:

receiving the data from a source (host system 12 of Fig. 1) (col. 3, ll. 1-6);

storing the data in a plurality of blocks having a length of 2^n, where n is a positive number (col. 5, ll. 13-26), wherein data inputted is stored in the memory segment of the DRAM specifically for data blocks, having the block size of 2^7=128 bytes, wherein n=7;

adding padding to the last received data to ensure the data is of a fix length (col. 4, ll. 42-50);

calculating a first cyclical redundancy code (CRC) for each of said plurality of blocks (col. 4, ll. 24-27), wherein the first CRC corresponds to the ECC check symbols calculated;

storing the first CRC in a second memory on said buffering device (col. 5, ll. 13-26), wherein the first CRC corresponds to the ECC check symbols are stored in a different segment of the DRAM from where the data blocks are stored;

a second port (Fig. 1), wherein the second port is the interconnection between the memory system (Fig. 1, ref. 10) and the data storage system (Fig. 1, ref. 14); and

when writing said data to said second port, computing a second CRC for each of said plurality of blocks and if said second CRC corresponding to a given block is equal to said first CRC corresponding to said given block, writing said given block to said second port (col. 9, ll. 22-48).

Jaquette is analogous art because Jaquette is in the field of applicant's endeavor, which would be related to CRC being utilized in association with control of data transferring.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Jaquette's protection of data as the data passes through the buffering device into O'Grady's data buffering system and method. The resulting combination of the references further teaches the method and the computer program product for protecting data as it passes through the buffering device that connects protocols that use different block sizes or unblocked data, comprising:

wherein each one of the plurality of blocks of storage have the length of 2^n, where n is a positive integer;

if the transfer length of the receiving packet (i.e. data) terminated prior filling the block of storage (i.e. not filling the end one of said plurality of blocks having the end cell of the transferring packet) of the plurality of storages, padding are added to fill up the block of storage of the plurality of storages (i.e. filling up the length of 2^n), therefore padding would be only added to the end one of said plurality of blocks that have the last

cell of the transferring packet (i.e. end of said transfer length of the packet) until the block of storage is full (i.e. end one of the plurality of block is complete);

as each cells of the data is being stored into the plurality of blocks, calculate the CRC for each of the cells being stored into each of the plurality of blocks;

storing the calculated final CRC in the second memory on said buffer device as the first CRC; and

when writing said data to the second port, computing the second CRC for each of said plurality of blocks and if said second CRC corresponding to the given block is equal to said first CRC corresponding to said given block, writing said given block to said second port.

The suggestion/motivation for doing so would have been for the benefit of ensuring the temporary stored data be transferred at high speed, without stopping, and be correct, without errors, when transferring (Jaquette, col. 1, ll. 22-24).

Therefore, it would have been obvious to combine Jaquette with O'Grady for the benefit of ensuring the temporary stored data be transferred at high speed, without stopping, and be correct, without errors, when transferring to obtain the invention as specified in claims 1 ad 12.

Fish teaches a system and a method comprising implementing a write command for a data wherein the CRC is calculated during the writing and the calculated CRC is written at the end of the data (col. 11, l. 65 to col. 12, ll. 4).

O'Grady as modified and Fish are analogous art because they are from the same field of endeavor as they are both associated with the control of data transferring for a computer system.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Fish's calculation of CRC into O'Grady and Jaquette's data buffering system. The resulting combination of the references further teaches the data buffering system comprising:

the CRC is calculated during the writing of each cell of the data into the plurality of blocks, therefore calculating the running CRC for the cells; and

when writing the cells to each one of the plurality of blocks is completed as the packet is completely written into the memory, the final calculated CRC would be written into the second memory on said buffer device as the first CRC.

The suggestion/motivation for doing so would have been of decreasing the time required for a number of different operations to be performed (Fish, col. 2, ll. 18-20).

Therefore, it would have been obvious to combine Fish with O'Grady and Jaquette for the benefit of decreasing the time required for a number of different operations to be performed to obtain the invention as specified in claims 1 and 12.

6. As per claim 4, O'Grady, Jaquette and Fish teach all the limitations of claim 1 as discussed above, where O'Grady and Jaquette further teach the method comprising wherein one of said first and said second ports is connected to a protocol that does not

use fixed block lengths (Jaquette, col. 4, ll. 42-50 and O'Grady, col. 1, ll. 23-25), as the receiving data have different lengths.

7. As per claim 5, O'Grady, Jaquette and Fish teach all the limitations of claim 1 as discussed above, where Jaquette further teaches the method comprising wherein locations in said second memory are mapped to locations in said first memory (Jaquette, col. 5, ll. 26-37), wherein the mapping is implemented utilizing an offset from the data block partitions.

8. As per claim 14, O'Grady, Jaquette and Fish teach all the limitations of claim 12 as discussed above, where Jaquette further teaches the computer program product stored on a computer readable medium to be executed comprising wherein said computer program product is embodied on a protocol interface device (Jaquette, Fig. 1, ref. 10, 16) connected between a bus and a tape drive (e.g. magnetic tape) (Jaquette, col. 4, ll. 8-13), wherein the bus is the interconnection between the host system (Jaquette, Fig. 1, ref. 12) and the memory system (Jaquette, Fig. 1, ref. 10) and the data storage system (Jaquette, Fig. 1, ref. 14) may be a magnetic tape.

9. Claims 2 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Grady et al. (US Patent 6,757,791) in view of Jaquette et al. (US Patent 6,009,547) and Fish et al. (US Patent 4,241,420) as applied to claims 1 and 12 above, and further in view of Hogan et al. (US Patent 6,765,739).

O'Grady, Jaquette and Fish teach all the limitations of claims 1 and 12 as discussed above, where Jaquette further teaches the method comprising checking the data with ECC for error (Jaquette, col. 6, ll. 46-59).

O'Grady, Jaquette and Fish do not teach the method comprising wherein the data is received with a protection code that is checked and discarded.

Hogan teaches a system and a method comprising receiving an encoded data (Fig. 2, ref. 32) (i.e. protection code) and removing (i.e. discard by removing) the ECC from the received encoded data (Fig. 2, ref. 36).

Hogan is analogous art because Hogan is in the field of applicant's endeavor, which would be related to the use of error correction code in association with data transferring.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Hogan's receiving and removing ECC from received data into O'Grady, Jaquette and Fish's method. The resulting combination of the references teaches the method further comprising wherein the data received is encoded with ECC (i.e. protection code) and the checking and removing of the ECC.

The suggestion/motivation for doing so would have been for the benefit of providing copy protection data to be written onto the data storage system such as a disk (Hogan, col. 3, ll. 27-45).

Therefore, it would have been obvious to combine Hogan with O'Grady, Jaquette and Fish for the benefit of providing copy protection data to be written onto the data storage system such as a disk to obtain the invention as specified in claims 2 and 13.

10. Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Grady et al. (US Patent 6,757,791) in view of Jaquette et al. (US Patent 6,009,547) and Fish et al. (US Patent 4,241,420) as applied to claim 1 above, and further in view of "PCTechGuide".

O'Grady, Jaquette and Fish teach all the limitations of claim 1 as discussed above, where Jaquette further teaches the method comprising wherein said buffering device is a DRAM device (Jaquette, Fig. 2, ref. 16) connected between a bus and a tape drive (Jaquette, data storage device 14 of Fig. 1) (Jaquette, col. 4, ll. 8-13), wherein the bus is the interconnection between the host system (Jaquette, Fig. 1, ref. 12) and the memory system (Jaquette, Fig. 1, ref. 10) and the data storage system (Jaquette, Fig. 1, ref. 14) may be a magnetic tape. But, O'Grady, Jaquette and Fish does not teach the method comprising wherein the DRAM device is a DDR device.

PCTechGuide teaches a system and a method comprising transferring data utilizing DDR DRAM (DDR DRAM Section, 2nd paragraph on page 3).

O'Grady as modified and PCTechGuide are analogous art because they are from same field of endeavor as they are both associated with the use of DRAM.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include PCTechGuide's DDR DRAM into O'Grady, Jaquette and Fish's memory system.

The suggestion/motivation for doing so would have been for the benefit of allowing data to be transferred faster as data can be transferred during both the rising

edge and falling edge of the clock (DDR PCTechGuide, DDR DRAM Section, 2nd paragraph on page 3).

Therefore, it would have been obvious to combine PCTechGuide with O'Grady, Jaquette and Fish for the benefit of allowing data to be transferred faster as data can be transferred during both the rising edge and falling edge of the clock to obtain the invention as specified in claim 3.

11. Claims 7-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Grady et al. (US Patent 6,757,791) in view of Jaquette et al. (US Patent 6,009,547), Fish et al. (US Patent 4,241,420) and Malakapalli et al. (US Patent 6,467,060).

12. As per claim 7, O'Grady teaches a device for buffering data comprising:

a first port (Fig. 1 ref. 111) and a second port (Fig. 1-2, ref. 112) utilized for communication (Fig. 1-2);

a plurality of blocks of storage (Fig. 2, ref. 161) that have been allocated for storing a transfer length of unblocked data (Abstract; col. 1, ll. 23-29; col. 1, l. 63 to col. 2, l. 17 and col. 6, ll. 36-43), wherein the packet (Fig. 2, ref. 113) of different transfer length are received, disassembled into cells to be stored into the plurality of blocks of storage as allocated;

a memory (Fig. 2, ref. 160) including said plurality of blocks (Fig. 2, ref. 161) for storing said data (packet 113 of Fig. 1-2) that is passing between said first port and said

second port, said data being written to successive ones of said plurality of blocks as said data is received until an end one of said transfer length is reached (col. 1, l. 63 to col. 2, l. 17; col. 6, ll. 36-43 and col. 6, l. 47 to col. 7, l. 8), as the packets of different length are received, disassembled into cells and stored (i.e. written) into the corresponding first-in-first-out (FIFO) queues in the plurality of blocks successively till the end of the packet.

O'Grady does not teach the device for buffering data between two protocols, at least one of which does not utilize blocks, said device comprising:

the first port connected to communicate using a first protocol of said two protocols;

the second port connected to communicate using a second protocol of said two protocols;

a cyclical redundancy code engine connected to be selectively connected to one of said first port and said second port;

the memory is a first random access memory connected to said cyclical redundancy code engine, wherein each one of said plurality of blocks in the memory have a fix size;

if an end one of said plurality of blocks that includes an end of said transfer length is not full of data, adding padding to said end one of said plurality of blocks until said end one of said plurality of blocks is completed, wherein padding is added only to an end one of said plurality of blocks that includes an end of said transfer length until the end one of the plurality of block is complete;

said cyclical redundancy code engine calculating a running cyclical redundancy code (CRC) for each one of said plurality of blocks as data is written to each one of said plurality of blocks;

a second random access memory connected to said cyclical redundancy code engine for storing for each one of said plurality of blocks, a final value of said running CRC that was calculated for each one of said plurality of blocks as a first CRC when writing to each one of said plurality of blocks is completed; and

a comparator connected to compare a second CRC calculated for each one of said plurality of blocks with said first CRC calculated when writing to each one of said plurality of blocks is completed.

Jaquette teaches a data protection device for buffering data between two protocols, at least one of which does not utilize blocks (col. 4, ll. 8-50, wherein one protocol conforms to a host system and the other protocol conforms to a data storage system and the protocol associated with the host system does not utilize blocks as data received from the host system may need to be padded to form blocks), said device comprising:

a first port connected to communicate using a first protocol of said two protocols (Fig. 1), wherein the first port is the interconnection between the memory system (Fig. 1, ref. 10) and the host system (Fig. 1, ref. 12), conforming to the protocol utilized by the host system;

a second port connected to communicate using a second protocol of said two protocols (Fig. 1), wherein the second port is the interconnection between the memory

system (Fig. 1, ref. 10) and the data storage system (Fig. 1, ref. 14), conforming to the protocol utilized by the data storage system;

a cyclical redundancy code engine (CRC generator circuit 20 of Fig. 1) connected to be selectively connected to one of said first port and said second port (col. 4, ll. 24-27 and col. 10, ll. 9-23), as the cyclical redundancy code (CRC) for each of the data inputted from each of the respective port is generated by the CRC generator circuit, therefore the CRC generator circuit is selectively coupled to the respective port, depending on which port is inputting data;

a first random access memory (Fig. 1, ref. 16) connected to said cyclical redundancy code engine (Fig. 1, ref. 20) and storing data in the first random access memory's plurality of blocks having a fix length of 2^n, where n is a positive number (col. 5, ll. 13-26), wherein data inputted is stored in the memory segment of the DRAM specifically for data blocks, having the block size of 2^7=128 bytes, wherein n=7;

adding padding to the last received data to ensure the data is of a fix length (col. 4, ll. 42-50);

calculating a first CRC for each of said plurality of blocks (col. 4, ll. 24-27), wherein the first CRC corresponds to the ECC check symbols calculated;

a second random access memory (Fig. 1, ref. 16) connected to said cyclical redundancy code engine (Fig. 1, ref. 20) for storing the first CRC in a second memory on said buffering device (col. 5, ll. 13-26); and

when writing said data to said second port, computing a second CRC for each of said plurality of blocks and if said second CRC corresponding to a given block is equal

to said first CRC corresponding to said given block, writing said given block to said second port, therefore the data passed through said device is protected by a CRC (col. 9, ll. 22-48).

Jaquette is analogous art because Jaquette is in the field of applicant's endeavor, which would be related to CRC being utilized in association with control of data transferring.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Jaquette's data protection for buffering data into O'Grady's data buffering system and method. The resulting combination of the references further teaches the device for buffering data between two protocols, at least one of which does not utilize blocks, said device comprising

a first port and a second port utilized for communication, wherein the first port connected to communicate using the first protocol of said two protocols and the second port connected to communicate using the second protocol of said two protocols;

the CRC generator circuit (i.e. cyclical redundancy code engine) selectively connected to one of said first port and said second port;

the memory is the first random access memory connected to said CRC generator circuit, wherein each one of said plurality of blocks in the memory have a fix size (e.g. 2^7=128 bytes block size);

if the transfer length of the receiving packet (i.e. data) terminated prior filling the block of storage (i.e. not filling the end one of said plurality of blocks having the end cell of the transferring packet) of the plurality of storages, padding are added to fill up the

block of storage of the plurality of storages (i.e. filling up the length of 2^n), therefore padding would be only added to the end one of said plurality of blocks that have the last cell of the transferring packet (i.e. end of said transfer length of the packet) until the block of storage is full (i.e. end one of the plurality of block is complete);

as each cells of the data is being stored into the plurality of blocks, calculate the CRC for each of the cells being stored into each of the plurality of blocks;

storing the calculated final CRC in the second memory on said buffer device as the first CRC; and

when writing said data to the second port, computing a second CRC for each of said plurality of blocks and if said second CRC corresponding to the given block is equal to said first CRC corresponding to said given block, writing said given block to said second port, therefore the data passed through said device is protected by the CRC.

The suggestion/motivation for doing so would have been for the benefit of ensuring the temporary stored data be transferred at high speed, without stopping, and be correct, without errors, when transferring (Jaquette, col. 1, ll. 22-24).

Therefore, it would have been obvious to combine Jaquette with O'Grady for the benefit of ensuring the temporary stored data be transferred at high speed, without stopping, and be correct, without errors, when transferring to obtain the invention as specified in claim 7.

Fish teaches a system and a method comprising implementing a write command for a data wherein the CRC is calculated during the writing and the calculated CRC is written at the end of the data (col. 11, l. 65 to col. 12, ll. 4).

O'Grady as modified and Fish are analogous art because they are from the same field of endeavor as they are both associated with the control of data transferring for a computer system.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Fish's calculation of CRC into O'Grady and Jaquette's data buffering system. The resulting combination of the references further teaches the data buffering system comprising:

the CRC is calculated during the writing of each cell of the data into the plurality of blocks, therefore calculating the running CRC for the cells; and

when writing the cells to each one of the plurality of blocks is completed as the packet is completely written into the memory, the final calculated CRC would be written into the second memory on said buffer device as the first CRC.

The suggestion/motivation for doing so would have been of decreasing the time required for a number of different operation to be performed (Fish, col. 2, ll. 18-20).

Therefore, it would have been obvious to combine Fish with O'Grady and Jaquette for the benefit of decreasing the time required for a number of different operations to be performed to obtain the invention as specified in claims 1 and 12.

Malakapalli teaches a system and a method comprising a comparator (Fig. 13, ref. 1370) to compare the first CRC to the second CRC (col. 16, ll. 33-37).

Malakapalli is analogous art because Malakapalli is in the field of applicant's endeavor as Malakapalli is related to the use of CRC.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Malakapalli's comparator into O'Grady, Jaquette and Fish's memory system.

The suggestion/motivation for doing so would have been for the benefit of increasing the integrity of data stored on mass-storage (Malakapalli, col. 3, ll. 35-41).

Therefore, it would have been obvious to combine Malakapalli with O'Grady, Jaquette and Fish for the benefit of increasing the integrity of data stored on mass-storage to obtain the invention as specified in claim 7.

13. As per claim 8, O'Grady, Jaquette, Fish and Malakapalli teach all the limitations of claim 7 as discussed above, where Jaquette further teaches the device comprising wherein said cyclical redundancy codes are stored in said second random access memory in a mapped relationship to said fixed size blocks stored in said first random access memory (Jaquette, col. 5, ll. 26-37), wherein the mapped relationship is implemented utilizing an offset from the data block partitions.

14. As per claim 10, O'Grady, Jaquette, Fish and Malakapalli teach all the limitations of claim 7 as discussed above, where Jaquette further teaches the device comprising

wherein locations in said second random access memory are mapped to locations in said first random access memory (Jaquette, col. 5, ll. 26-37), wherein the mapping is implemented utilizing an offset from the data block partitions.

15. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Grady et al. (US Patent 6,757,791) in view of Jaquette et al. (US Patent 6,009,547), Fish et al. (US Patent 4,241,420) and Malakapalli et al. (US Patent 6,467,060) as applied to claim 7 above, and further in view of Hogan et al. (US Patent 6,765,739).

O'Grady, Jaquette, Fish and Malakapalli teach all the limitations of claim 7 as discussed above, where Jaquette further teaches the device comprising checking the data with ECC for error (col. 6, ll. 46-59).

O'Grady, Jaquette, Fish and Malakapalli do not teach the device comprising a protection module connected to said first port for checking a protection code that is received and discarding said protection code.

Hogan teaches a system and a method comprising receiving an encoded data (Fig. 2, ref. 32) (i.e. protection code) and removing (i.e. discard by removing) the ECC from the received encoded data (Fig. 2, ref. 36).

Hogan is analogous art because Hogan is in the field of applicant's endeavor, which would be related to the use of error correction code in association with data transferring.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Hogan's receiving and removing ECC from received data

into O'Grady, Jaquette, Fish and Malakapalli's device. The resulting combination of the references teaches the device further comprising wherein the data received is encoded with ECC (i.e. protection code) and the checking and removing of the ECC, therefore, it would be obvious to have the protection module for implementing the functions just described.

The suggestion/motivation for doing so would have been for the benefit of providing copy protection data to be written onto the data storage system such as a disk (Hogan, col. 3, ll. 27-45).

Therefore, it would have been obvious to combine Hogan with O'Grady, Jaquette, Fish and Malakapalli for the benefit of providing copy protection data to be written onto the data storage system such as a disk to obtain the invention as specified in claim 9.

VI. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-5, 7-10 and 12-14 have received a final action on the merits. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

May 03, 2007

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

DONALD SPARKS
SUPERVISORY PATENT EXAMINER